C-17 WARNING AND CAUTION COMPUTER

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C-17 WARNING AND CAUTION COMPUTER (WACC)

OVERVIEW

The Warning and Caution Computer (WACC), Figures 1A Front, 1B Rear and 1C Top, is part of the C-17 integrated overall Warning and Caution System (WACS) that accepts discrete data, and data from 1553B bus connected specialized peripheral Line Replaceable Units (LRUs). Data transmission within the system is accomplished with a dual redundant MIL-STD 1553B serial data bus. WACC processed data is distributed to the overhead Warning and Caution Panel (WAP) via the 1553B. In addition, the WACC provides direct outputs to drive other annunciator lamps in the cockpit.

Included in the Warning and Caution System, Figure 2, is the Central Aural Warning System (CAWS) which provides audio warning derived from a menu of stored messages. As can be seen in Figure 2, the CAWS is architecturally located on the Mission 2 bus. The connection to, and the formatting of data from the WACS 1553B bus to the Mission 2 bus, is accomplished via the #2 Aircraft / Propulsion Data Management Computer (APM–2).

The Warning and Caution System consists of two redundant WACCs, a Warning and Caution Panel (WAP), and specialized Line Replaceable Units (LRUs) dedicated to the various aircraft operational systems noted below. One Warning and Caution Computer (WACC) serves as the 1553B Bus Controller (BC) while the redundant WACC serves as the Back Up Bus Controller. To further enhance the WACS reliability, the redundant WACC is powered by a separate 28 Volt power source.

The electronics suite, Figure 2, of the integrated Warning and Caution System consists of, but is not limited to, the following systems:

a. ANTI SKID/BRAKE TEMPERATURE COMPUTER (ABC)

b. FUEL QUANTITY COMPUTER (FQC)
c. FUEL SYSTEM MODULE (FSM)
d. PROXIMITY COMPUTER (PX)
e. ON BOARD INERT GAS GENERATION SYSTEM (OBG)
f. PROPULSION DATA MANAGEMENT COMPUTER (APM)
g. HYDRAULIC CONTROL UNIT (HCU)
Figure 2. Warning and Caution System Serial Bus Architecture

h. HYDRAULIC SYSTEM MODULE (HSM)
i. FLIGHT RECORDER (FDR)
j. WARNING AND CAUTION PANEL (WAP)
k. ENVIRONMENTAL SYSTEM MODULE (ESM)
l. AERIAL DELIVERY SYSTEM (ADS)
m. CENTRAL AURAL WARNING (CAW) (Connected to #2 Mission Bus)
n. WARNING AND CAUTION COMPUTER (WACC)

Each of the sub-systems noted above provide warning data to the WACC over the 1553B dual redundant data bus.

The Warning and Caution System link to the triply redundant mission system is via the Aircraft Propulsion Data Management Computers (APM) which are also redundant. Each APM is connected to the WACS 1553B bus and each provides a link to one of the mission system dual redundant buses acting as a Remote Terminal (RT). The mission buses consist of two dual redundant, independent 1553B data buses. The Central Aural Warning System (CAW) is also connected to the #2 Mission Bus.

The purpose of the separation of mission buses from the warning data bus system is to maintain isolation, and to reduce interdependence between the systems.

PHYSICAL ATTRIBUTES

The WACC is designed as a fully modular chassis with defined, independently testable, modules. A block diagram is shown in Figure 3. The present module population consists of 8 modules, not including power supply, with two spare module slots available for growth. The module configuration includes:

a. 1750A CPU Module
b. Memory Module
c. 1553B Module
d. Discrete Multiplex Modules (5 of identical design)
e. Power Supply
f. Spares (2)

The WACC is housed in a standard 3/4 ATR enclosure and weighs 17.8 lbs. Nominal power input to the internally mounted 28 Volt switching regulator is less than 24 Watts. Discrete input bias is sourced by the aircraft 28 Volt bus at 3 milliamperes provided per discrete. All modules are of the 6 inch by 9 inch form factor. A DMX module, 1 of 5 identical modules, is shown in Figure 4.

The totally modular approach to the design of the WACC allows system upgrades in hardware with minimum or no impact to the existing Shop Replaceable Units (SRUs) suite.

INPUTS AND OUTPUTS

Each WACC services 385 discrete signals consisting of predominantly ground enabling signals with sensor bias supplied by the WACC. A small number of input discretes are high level (+28 volt discretes). Of the 385 discretes, 87 are presently defined as spares. All of the discretes are fully protected against high electrical pulse fields e.g. lightning, with high energy absorbing discrete transient protectors. Each WACC also provides 15 fully fault protected current sinks which are utilized to drive caution and advisory indicators directly.

Sufficient signal detection margin is designed into the input signal conditioning circuitry such that proper sensing of the inputs is achieved even with one WACC powered down.

WACC FUNCTIONAL REQUIREMENTS

The Computer Software Configuration Items (CSCIs) initiate instructions that execute acquisition and processing of direct and 1553B bus inputs and control the display of fault annunciations. The unit performs the bus controller or back up bus controller function and controls periodic and initiated Built In Test (BIT).

The following Computer Software Configuration Items (CSCIs), define the majority of processing modules:

- Computer Power Interruption,
- Initialization,
- Power On Built-In-Test (BIT),
- Input 1553B Data,
- Output 1553B Data,
- Computer Health Monitor (Watch Dog Timer),
- 1553B Bus Fault Management,
- Mode of Operation,
Figure 3. Warning and Caution Computer Functional Block Diagram

- Initiated BIT,
- Annunciation Control,
- Foreground/Background,
- Periodic BIT,
- Interrupt Handlers.

The core of the functional processing elements are contained in the Attribute Table (AT). This table contains the matrix map of all algorithms required to process the related discrete inputs which may be input directly to the WACC or obtained from the 1533B data bus from a peripheral subsystem.

Figure 4. DMX Module

The result of the processing of any AT algorithm is the control of the Master Caution or Master Warning annunciator and the display of the appropriate message on the Warning Annunciator Panel (WAP). If applicable, an aural message will be initiated by the Central Aural Warning System.

An example of a minor equation of the AT is a display failure of the Multi Function Display #1 (MFD):

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>a) MFD #1 INOP</td>
<td>1553B APM1</td>
</tr>
<tr>
<td>b) MFD #1 INOP</td>
<td>1553B APM2</td>
</tr>
<tr>
<td>c) MFD #2 INOP</td>
<td>1553B APM1</td>
</tr>
<tr>
<td>d) MFD #2 INOP</td>
<td>1553B APM2</td>
</tr>
</tbody>
</table>

Algorithm = (a OR b) AND (NOT(c OR d))

If APM#1 or APM#2 reports a failure of MFD#1 and MFD#2 reports OK from APM#1,2, then send “True” to the Master Caution annunciator and WAP displays the message “MFD 1”.

1750A CENTRAL PROCESSING UNIT (CPU)

The 1750A Module Single Board Computer (SBC), contains all resources necessary to meet 1750A processing requirements. The SBC contains Memory Management to address local and extended memory. The SBC onboard memory complement includes 32 Kwords of boot/diagnostic EPROM memory, 32 Kwords of EEPROM program memory, and 32 Kwords of RAM data memory. The Boot/ Diagnostic Memory overlays the lower 32 Kword main program memory and is selected via a control discrete generated by the sequencing logic of the power supply when a “Cold Start” is initiated.

Address locations from 00000H to 0FFFF (Decimal 0 to 65,535) are located on the SBC while memory locations 10000H to 57FFFH (Decimal 65,536 to 360,447) are addressable on the Memory Module. Locations 58000H to 0FFFFH (Decimal 360,448 to 1,048,575) are
addressable by the Memory Management Function and may be utilized to access memory on either or both of the spare growth slots within the WACC.

In addition to the 1750A CPU and memory complement noted above, the SBC contains the following functions:

- Clock generator,
- Wait state generator,
- Watch-dog timer
- Configuration register
- Address decoding
- Bus interfaces,
- Discrete I/O Ports
- RS232C asynchronous data link
- DMA interfaces.

The CPU interfaces with on board peripheral components (Local Bus) and off board resources (System Bus) over two distinct buses. This is to allow the CPU to operate at higher throughput (0 or 1 wait state) when accessing resources on board. The present configuration processes data at about 1 MIPS (Millions Of Instructions Per Second). An update, pin compatible, 1750A Module CPU, will process data at over 2 MIPS. Processor speed options to 6 MIPS are available.

System upgrades to date include the replacement of EPROMS (ultra violet erasable memory with EEPROMS which are electrically alterable in the circuit environment. The EEPROMS may be reprogrammed via the RS232 serial test data link.

**MEMORY MODULE**

The memory module provides additional system memory for the 1750A CPU environment. The block diagram, Figure 5, shows that the memory is partitioned into three unique regions consisting of: 32 KWords Electrically Erasable Memory (EEPROM), 224 Kwords of configurable memory which may be Random Access Memory (RAM), Ultra Violet Erasable Memory (UVPROM), or EEPROM and 512 Words of Non Volatile Vertically Integrated Random Access Memory (NOVRAM).

The first 32 Kwords of EEPROM are dedicated to program requirements. The present WACC configuration utilizes 16 KWords of this region of memory. EEPROM memory is programmed while the memory module is installed in the WACC via the RS232C serial link resident on the 1750A Module.

The configuration of the 224 Kword region of memory is determined by on board connections. This region of memory is populated in the current WACC configuration.

The NOVRAM memory consists of a static random access memory vertically integrated on the die over an area of memory which acts similar to that of an EEPROM. Information contained within the RAM, upon command e.g., Power shut down, is copied into the non-volatile portion of the memory and in this way critical system data is retained during periods of system shut down or power failure. This memory can be interrogated by maintenance personnel when analyzing system performance.

**1553B BUS INTERFACE MODULE**

The 1553B bus interface module, Figure 6 Block Diagram, is designed so that operation as a Bus Controller (BC) or Back Up Bus Controller (BBC) is possible. The module is designed to provide full MIL-STD-1553B multiplex data bus control for the C-17A Warning and Caution System.

Both BC and BBC have discrete interfaces to communicate to each other health and status information, so that a hand over to the BBC can
be accomplished in the event of a failure. This is in addition to the usual method of failure detection with 1553B software and firmware.

The prime components of the module consists of dual transformer coupled transceivers, 2 KWords of dual port RAM, and two hybrids which serve as a data formatter, checker and interface.

**DISCRETE MULTIPLEX MODULE**

The Discrete Multiplex Module (DMX), Figure 7 Block Diagram, provides the signal conditioning and state determination for 77 discrete input signals and 3 current sinks utilized to drive outboard caution and warning incandescent displays. Thus the present WACC can accept 385 discrete signals, and can provide outputs to 15 lamp drivers.

In addition to the software filtering of the monitored discrete, an RC filter is included in each discrete line to reduce the susceptibility to transients and inevitable contact bounce from mechanical sensors.

All of the input and output lines of the module are protected against externally induced transients, and in addition the lamp driver circuits are protected against shorts and inadvertent direct connections to the +28 volt power bus.

**BUILT IN TEST (BIT)**

Built In Test (BIT) operates in two independent modes consisting of Periodic BIT and a Maintenance Bit. Periodic BIT monitors the WACC during normal operation while Initiated BIT shall be usable only when the aircraft in on the ground (Weight On Wheels – True). The BIT modes are utilized to detect functional degradation and component failure. Failure data taken during operational mode (Periodic BIT) is stored in Non Volatile Memory (NVRAM) for later readout and analysis by maintenance personnel.

DMX Built In Test (BIT) is included on each assembly. The BIT function consists of two parts: The first test consists of a check of each of the eleven analog multiplexers. This is accomplished by providing a reference voltage to each multiplexer, utilizing the eighth channel of each device, and then detecting the state of the comparator circuit. The second test is implemented by forcing each of the remaining 7 channels of each multiplexer alternately to both a low state (Logic 0) and high state (Logic 1) and again monitoring the output of the comparators.

**SYSTEM ENHANCEMENTS**

In process studies include high level integration of the Discrete Input/Output processing circuitry utilizing Application Specific Integrated Circuits (ASICs) and methods, both hardware, firmware and software, for reducing system cost and increasing system throughput.

**WACC GROWTH TO DATA ACQUISITION SYSTEM**

The design modularity of the system allows usage of the system for other applications (growth) within the C-17 environment and is additionally applicable to other tasks where data acquisition, formatting, and processing is required. See Figure 8, Expansion of the existing system to acquire and process data may be accomplished by removing one or more of the DMX Modules and replacing it with a linear data acquisition module that could contain analog-to-digital and digital-to-analog Conversion.

To further enhance utility within the C-17 environment, a reconfigured DMX containing other processing elements can be implemented in a plug compatible module with new inputs and outputs utilizing many of the 87 existing spare wired discrete inputs. These spares are conduits to interface new signals to the WACC. The spare inputs are distributed over the five DMX Modules.

No backplane changes are necessary for the above noted expansion. The WACC computer, has in addition to the 8 previously defined modules, two spare slots, with the dedicated backplane wired with all required 1750A address, data, and control signals. These slots can
Figure 7. DMX Block Diagram

Figure 8. WACC Growth Potential
provide additional system expansion. With minor backplane modifications to accommodate special cabling requirements, the WACC can provide enhanced system capability in the following data processing areas: Expert systems (Neural, DSP, Fuzzy Logic), Linear Inputs/Outputs and Synchro/Resolver Inputs/Outputs. An 8 MByte incident (hindsight) recorder (IREC) may be installed into one of the spare modules slots. Contents of the IREC may be downloaded to a portable test set via the test port RS232 serial data link, when the aircraft is on the ground.

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GLOSSARY
ASIC Application Specific Integrated Circuit
AT Attribute Table
BC 1553B Bus Controller
BBC 1553B Backup Bus Controller
BIT Built In Test
CSCI Computer Software Configuration Items
DMX Discrete Input Multiplex Module
IREC Incident Recorder
LRU Line Replaceable Unit
MFD Multi Function Display
RT Remote Terminal

WACC Warning and Caution Computer
WACS Warning and Caution System

BIOGRAPHY
Gerald Lewis received his MS and BS degrees in Electrical engineering from the University of Connecticut in 1969 and New Haven University 1966 respectively.

His areas of expertise includes: Data acquisition systems architectures and analysis, development and analysis of Fault Tolerant Systems, and reverse engineering and simplification of discrete component systems by integration into custom and semi-custom integrated circuits. In addition to having a strong background in analog, digital, and firmware design, Mr Lewis is knowledgeable in applying radiation hardening techniques at the hardware and system level.

In his present position at Teledyne Systems since 1977, he has been involved in system architectures and hardware development of the F-18 fault tolerant seat ejection system (NACES), a fault tolerant armament system controller for the preset and launch of torpedoes and other weapons for the CV-Helo and other aircraft, and several airborne communications systems. His present assignment is the system and hardware upgrade for the C-17A Warning and Caution Computer described herein.

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