The principle of ERPD operation is shown in Figure 12.3.3. A tristate phase-frequency detector (PFD), shown in the upper branch of the figure, tracks small phase errors. When its error surpasses 180°, the pump-up signal PU is sampled high by the negative edge of the reference clock, generating a count-up signal CC. This increments a digital register, driving the DAC and causing it to add 180° of scaled current. Conversely, the reference input to the PFD is inverted, subtracting 180° from its operation. The sum of the DAC current and charge-pump may thus track an arbitrary mounting phase error while maintaining PFD operation within ±180°. The counting process causes as the loop settles and only the PFD and charge-pump are active in the steady state. Hysteresis of DAC stopping eliminates the need for precise matching of DAC and charge-pump currents.

The ΣΔPLL's large phase excursions demand attention to linearity in PFD logic and charge-pump. Residual nonlinearities fold noise-shaped phase error energy back into the baseline. A tristate PFD of conventional architecture uses differential logic for symmetry and noise immunity. Its resistive circuitry is crafted to suppress dead-zone gain variations as well as anomalies near 180° where the flip-flop clock input change level. The phase error between Pref and Pdir is represented by the difference between PFD outputs PU and PDI which drive the charge pump in Figure 12.3.4. The charge-pump core consists of multiple differential-pair current switches controlled by signals SU and SD. These signals are driven through multiplexers fed by buffered bias voltages arranged to provide minimal-swing, linearized driving waveform to minimize tailurrent transients. Simulations indicate that the circuits, with 1% matching of current sources, have sufficient linearity to reduce folded noise below the thermal noise levels of the current sources and loop filter.

The multi-modulus frequency divider shown in Figure 12.3.5 is composed of a divide-by-468 stage followed by three divide-by-25 stages [2]. It has a modulus range of 32 to 8294 increments of 2, and produces less than 0.4 parts per million (ppm) excess jitter in response to the 28 sequence. Register-loaded differential logic at the front end of the divide-by-468 block achieves 2.5GHz operation in the 0.15μm process. The divide-by-468 operation uses phase-shifting with glitch-free make-before-break switching, allowing robust operation over a much wider range of frequencies than the prior art [2, 4]. To minimize noise injection, all transistors are driven by the output of the divider through the OUT1 path. OUT2 path is used to achieve glitch-free switching between phases of 0 and 180°. The remaining divider blocks are implemented with full-swing, true single-phase clocked (TSPC) logic.

The synthesizer, integrated with a prototype HCMOS baseline transceiver ASIC in 0.5μm CMOS, is shown in Figure 12.3.8. The die is 4.30x4.53mm², of which 3.30mm² is occupied by the ΣΔFM synthesizer. Phase noise, shown in Figure 12.3.6, is -104dBc/Hz in-band, meeting specifications. An inset demonstrates performance with phase noise carrier modulation. The settling time shown in Figure 12.3.7 is <3μs. Saturated the baseline logic clock (25MHz) are 7.24μA. Power consumption for the synthesizer, excluding the offset VCO, is 3.4mA at 3.3V.

References:
Figure 12.3.1: Block diagram of the wideband FN synthesizer PLL.

$X_{mod} = x + (1 + 2.9842^2 + 2.9692^2 + 0.984^2) e$

Figure 12.3.2: Ideal phase error transients of type-1 and type-2 PLLs.

Figure 12.3.3: The extended-range phase detector concept.

Figure 12.3.4: Charge pump schematic.

Figure 12.3.5: The high speed multi-modulus divider.

Figure 12.3.6: Unmodulated carrier spectrum (receive mode, 2310MHz) and modulated FSK eye diagram (transmit mode, 2430MHz).

Figure 12.3.7: See page 457.
Figure 12.3.8: See page 457.