RF Power Amplifier Integration in CMOS Technology

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ABSTRACT
This paper explores different levels of integration for CMOS RF power amplifiers, including integration fully on chip, integration with LTCC passive components, and integration with off-chip components. At 1.9GHz, the fully on-chip integrated CMOS PA can deliver 20 dBm output power with 16% efficiency. Because the LTCC inductors have much higher Q than the on-chip inductors, the CMOS PA integrated with passive components embedded in LTCC can improve the output power and efficiency to 24 dBm and 32% at 1.9GHz, respectively. The 2.4GHz Bluetooth PA with discrete passive components for output matching exhibits 22 dBm output power and 44% efficiency. To our knowledge, this paper reports the first development of fully on-chip integrated and LTCC hybrid CMOS power amplifiers.

INTRODUCTION
Most of RF power amplifiers (PA) are implemented in GaAs technology because of superior device performance. However, Si MOSFET continues to improve operation speed through downsizing, and CMOS has become viable option for RF PA implementation. Although CMOS PA's have been demonstrated operating at 800 MHz [1] and 1.9GHz [2], the issues about the integration of CMOS RF power amplifiers have not been addressed extensively.

The needs of highly integrated RFIC rise from the successful experience of digital IC because high levels of integration lead to compact size, short time-to-market, and cost reduction. The merits of integration can probably be applied to RFIC based upon the same arguments. However, digital IC is quite ready for the integration of system-on-chip, while RFIC is still often accompanied by many off-chip passive components. The major challenge for RFIC to achieve high levels of integration is the difficulty to implement high performance on-chip inductors in commercial IC processes. The quality factors (Q) of the on-chip spiral inductors in BiCMOS/CMOS technology are typically below 8 [3], and it is a well-known technical bottleneck to implement high performance integrated RF power amplifiers. Hence, all of the reported CMOS RF power amplifiers require off-chip baluns, capacitors, and inductors to match to single-end 50 ohm, as shown in table 1.

This paper discusses the development of CMOS RF power amplifiers integrated in three different levels: integration fully on chip, integration on LTCC (Low Temperature Co-fired Ceramics), and integration with discrete components. These three power amplifiers are designed for the wireless applications with constant-envelop modulation schemes, and, therefore, the design efforts are focused on output power and efficiency.
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Table 1. Summary of CMOS RF power amplifiers.

INTEGRATED POWER AMPLIFIERS

A. Fully integrated PA

The 3V monolithic fully integrated power amplifier (FIPA), operating at 1.9GHz, is implemented in a 0.8-um CMOS process. The configuration of the FIPA is two-stage common-source cascade as shown in Fig. 1. The pad parasitics are included during the PA design and simulation, but they are not shown in the schematic diagram. The first stage is designed to have maximum gain and the second stage is matched to have maximum efficiency. A differential architecture is considered due to its advantages of reducing the stress of breakdown voltage, increasing voltage swing headroom, and even harmonics cancellation. However, a low-loss balun is required for the differential PA to convert from differential to single-end output. If the loss of the balun is more than 3 dB, it will undermine most advantages of the differential topology. The difficulties of building a low-loss balun on Si make the differential topology not preferable.

All of the matching and tuning networks of the FIPA are accomplished on chip with MOS capacitors and spiral inductors. Both of the input and output are matched to 50 ohm, and the DC blocks are also incorporated into the input and output matching networks. The gate width of the first stage MOSFET is 1300 um and the second stage is 2800 um. The die photograph of the FIPA is shown in Fig. 2. For 3V operation, the FIPA delivers 24 dBm output power with 16% drain efficiency to the 50-ohm load as shown in Fig. 3.

![Fig. 1. The schematic diagram of the monolithic fully integrated power amplifier and LTCC hybrid power amplifier.](image1)

![Fig. 2. The photo of the fully integrated power amplifier.](image2)
B. LTCC hybrid PA

In addition to integration on chip, RF power amplifiers can also be fully integrated on package. It has been reported that the inductors built in LTCC technology have much better $Q$ than the spiral inductors in CMOS/BiCMOS technology [4,5]. To replace lossy on-chip inductors with high $Q$ LTCC inductors, part of the power amplifier circuit should be pushed down to LTCC.

The 1.9 GHz two-stage common-source cascaded LTCC hybrid PA (LTCC PA) is also implemented in a 0.8 um CMOS technology and its schematic diagram is similar to the one shown in Fig. 1. The two power transistors and the inter-stage matching network are implemented on chip, as shown within the shaded area in Fig. 1. The other circuits outside the shaded area are implemented on a 20-layer LTCC board. Both the input and output of the LTCC PA are matched to 50 ohm as well. The interconnections between the CMOS and LTCC circuits are through bondwires. For 3V operation, the LTCC PA can deliver 24 dBm to the 50-ohm load with 32% of drain efficiency as shown in Fig. 3.

C. PA with discrete components

A CMOS PA operating at 2.4GHz for Bluetooth application is implemented in a 0.24-um CMOS technology. The die photo of the Bluetooth PA is shown in Fig. 5. The topology of four-stage common-source cascade is used to boost the signal gain. The load contour of constant output power of the 30x50um MOSFET, measured with the fixed 50-ohm input impedance, is shown in Figure 6. The maximum output power and associated efficiency from load-pull measurement are 22 dBm and 44%, respectively. The output power and efficiency versus input power are shown in Fig. 7. In order to tune for high performance, the output network is composed of discrete inductors and capacitors. However, the input matching, inter-stage matching, and RF chokes are still implemented on-chip with spiral inductors and poly-insulator-poly capacitors to maintain high levels of integration.

CONCLUSIONS

Three CMOS RF power amplifiers of different integration levels are demonstrated. The fully on-chip integrated PA can achieve 20 dBm output power with 16% efficiency. The LTCC hybrid PA can improve the performance significantly by replacing the lossy on-chip inductors with high $Q$ inductors embedded in LTCC. At 1.9GHz, the LTCC PA can achieve 24 dBm output power and 32% efficiency. The Bluetooth PA with discrete
components for output matching can have 22 dBm output power and 44% efficiency at 2.4GHz. To the author's knowledge, this paper reports the first development of CMOS RF power amplifiers integrated fully on chip and with LTCC.

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Fig. 5. The die photo of the power amplifier for Bluetooth application.

Fig. 6. The constant output power contour of the MOSFET with 30x50um gate width.

Fig. 7. The measured output power and efficiency versus input power.

REFERENCES