A CMOS $g_m$-C IF Filter for Bluetooth

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Abstract

An 18th (4th + 14th) order $g_m$-C IF filter for the Bluetooth short-range radio, implemented in a 0.6μm CMOS process, is presented. The filter bandwidth is 1MHz, the center frequency $f_c$ is 3MHz, the in-band group delay variation is 0.75μs, and the stop-band attenuation at $f_c±1MHz$ is at least 47dB. The noise floor is 250μVRms, and the spurious free dynamic range is at least 58dB for out-of-band signals, thus exceeding the Bluetooth requirements. Current consumption is 2.4mA from a 2.5V power supply.

1. Introduction

One of the most challenging parts of a radio receiver is the channel filtering required to provide selectivity and robustness with respect to in-band blocking. The Bluetooth short-range radio specification [1] is relaxed to promote highly integrated designs, and in the following we study an integrated solution to the selectivity problem.

The in-band selectivity can be achieved either with analog filters, or with mixed analog-digital circuits, where the digital filters provide the close-in selectivity, and the blocking and anti-alias filtering is done in the analog domain. With the latter approach the requirements on and the complexity of the analog filters are minimized. The requirements on the A/D converter, however, will be tougher than dictated by the desired signal itself, as it must have a wide enough dynamic range to handle the first few adjacent channels where analog filters do not provide very high attenuation. Unless a zero-IF architecture is employed, the A/D converter must be able to resolve the desired signal with sufficient resolution in the presence of blocking signals. For Bluetooth we assume a carrier-to-noise ratio of 21dB for a 0.1% bit error rate, and the required blocking level is 40dBc, resulting in some 61dB A/D-converter dynamic range at a 1Ms/s symbol rate.

An analog approach, with all selectivity and blocking provided by an active on-chip IF filter, will require a sophisticated high-order IF filter. In a zero-IF receiver the selectivity filter will consist of two identical low-pass filters (i.e. one for each I and Q path). This does minimize filter complexity, but 1/f noise and LO leakage problems will severely limit the performance. Bluetooth specifically supports low-IF receivers with finite in-band image suppression (20dBc suppression), and exploiting this, one can design a band-pass filter with a center frequency around a few MHz (i.e. a few channels up with 1MHz channel spacing). If the IF frequency is higher than 2MHz, then no folding distortion will occur, should a coincidence detector be used (Bluetooth uses binary GFSK modulation). Further, 1/f noise is not a problem above a few hundred kHz even if an MOS technology is chosen for the filters. It is, however, desirable to keep the IF frequency as low as possible, as current consumption will be proportional to the center frequency. Accordingly, an IF of 3MHz has been chosen in this work.

On-chip devices have large absolute spreads but good matching properties. Assuming a 1% matching between large devices (which is conservative for the technology used), we expect a 30kHz offset on the nominal center frequency. This spread is small compared to the 1MHz channel width, and the entire IF filter can be automatically tuned by locking a VCO, built like one filter resonator stage, to a crystal reference. By exploiting this accurate matching no further tuning is necessary. If the VCO frequency is the same as the IF center frequency, mismatch will be minimized but an on-channel interferer will be present. Depending on the isolation properties of the chosen IC technology this may or may not be a problem. Alternatively, a larger mismatch can be tolerated and the VCO frequency be put off-channel. In the present work we have not implemented the auto-tuning, as the feasibility of this only depends on relative device mismatch, and the filter complexity itself requires matching of at least 1% to achieve the desired transfer function.

2. Filter design

The requirements on an analog low-IF band-pass filter can be split into dynamic range requirements and selectivity requirements. The dynamic range must be such that no blocking signals desensitize the receiver. The performance in presence of inter-modulation distortion is tested with a difference frequency of 3, 4, or 5MHz between a static sine wave signal and
a Bluetooth signal, and the required 3\textsuperscript{rd} order intercept point IP\textsubscript{3} must be 54dB above the -70dBm reference sensitivity level, or 75dB above the noise floor.

The selectivity requirements in Bluetooth are 0dB, 30dB and 40dB for interferers one, two, and three or more channels away, respectively. System simulations show that the filter should distort the amplitude and the phase of the in-band signal as little as possible. Preferably, the in-band group delay variation should be limited to below 1\mu s to avoid inter-symbol distortion. After evaluating the behavior of a large number of filters, the architecture of Fig. 1 was chosen. The filter is made of two cascaded blocks: a 4\textsuperscript{th} order band-pass Butterworth filter, followed by a 10\textsuperscript{th} order band-pass Butterworth filter where two pairs of transmission zeros have been introduced, to achieve an attenuation of at least 40dB already for the first interferers (i.e. for frequencies below 2MHz and above 4MHz). In this way, the filter can robustly tolerate the expected mismatches between components. The overall -3dB bandwidth coincides with the -3dB bandwidth of the first filter, as the second filter was designed with a bandwidth of 1.4MHz. This was to avoid the large group delay variation near the roll-off frequency of the higher order Butterworth filter.

The filter has been implemented with the \(g_m\)-C technique, where each inductance is replaced by a gyrator and a capacitance. The floating series of a capacitance and an inductance (such as the \(C_{L,2\alpha}\)-\(L_{2\alpha}\) pair and the \(C_{L,4\beta}\)-\(L_{4\beta}\) pair) and the \(C_{L,2\alpha}\)-\(L_{2\alpha}\)-\(R\) series are implemented as shown in Fig. 2. These circuits do not introduce any parasitic node in the filter design, which is especially useful if the transconductor used in the gyrators is itself without internal nodes. In such a case, the transition from passive prototype to active filter implementation is very straightforward, since there are no parasitic time constants affecting the circuit behavior, other than the distributed time constants in the channel of the MOS transistors.

It should be noted that capacitors \(C_{2\alpha}\) and \(C_{4\beta}\) cannot be gyrated without introducing parasitic nodes. To avoid this, we have chosen to implement \(C_{2\alpha}\) and \(C_{4\beta}\) as floating pMOS capacitors working in the depletion region. These capacitors will not track the other capacitors in the filter, but the spread in their value is low enough to be acceptable; furthermore, the final values of the transmission zeros were chosen after simulating the active filter in all process corners. Alternatively, transmission zeros could be implemented with cascaded notch stages, or the filter order could be increased. These options, while typically more robust (although a notch stage still introduces a parasitic node), would increase filter complexity, power consumption, and noise.

3. Transconductor design

Since the target application is in portable communications, the transconductor should display a large enough linear range while working at low power supply voltages (2-3 V). The balanced transconductor used in this work has been proposed by Nauta [2] and is reproduced in Fig. 3. Since the transconductor is built with inverters, it is very well suited for low voltage applications. We will briefly state, without proof, the major known features of the transconductor, assuming for simplicity that all inverters are identical. Clearly, the transconductor has no internal nodes. As long as all transistors are working in saturation, the transconductance of the circuit is a linear function (neglecting mobility variations of the charge carriers) of
the input voltage \( I_c - I_e = g_m (V_+ - V_-) \), where \( g_m \) is the inverter transconductance. The four inverters at the output of the stage \( I_4, I_4, I_5, I_5 \) provide both common-mode stability, and a high differential-mode output resistance. Originally, this transconductor was proposed for very high frequency (low-pass) applications. In such cases, transistors must often have short channels, which causes the parasitic output resistance of the transconductor to be low (a dc-gain of at least 40dB is required for a transconductor to be used in a \( g_m \)-C filter). A higher output resistance can be recovered by tuning the supply voltage of inverters \( I_4 \) and \( I_5 \) (Q-tuning). However, since the present application is not at high frequencies, we can afford to design long transistors \( L=5\mu m \), with a parasitic output resistance so high (in all process corners), that no Q-tuning is necessary. This is a considerable simplification in the filter design. Furthermore, since all transistors are long and large, matching between the various stages of the filter is excellent, which was verified through Monte Carlo simulations.

**Stability considerations.** Simulations of the active filter with a non-quasi-static model for the MOS transistors show that the design of the transconductors in an active LC parallel pair (Fig. 4) requires extra care. An analytic approach to the stability problem for such a circuit [3], when the distributed time constants in the transistor channels are taken into account, shows that the circuit is unstable, unless the dc-gain \( A_0 \) of the transconductors is very low \((A_0 \approx 19 \) for an unloaded LC pair). Thus, in a bandpass filter application, two instances of the same basic transconductor cell must be designed, one with \( A_0 \) as high as possible, and one with very low \( A_0 \). As a matter of fact, a low \( A_0 \) is easily obtained by lowering the \( g_m \) of inverters \( I_3 \) and \( I_5 \) (for instance, by reducing their width). \( A_0 \) is then given by the ratio \( g_m/A_{gm} \), where \( A_{gm} \) is the transconductance difference between \( I_4 \) (\( I_5 \)) and \( I_3 \) (\( I_5 \)). In this expression for \( A_0 \) we have neglected the parasitic output resistance of the transconductor, since it is much higher than \( 1/A_{gm} \). This fact makes the robust realization of a low \( A_0 \) possible, since the matching of \( g_m \) and \( A_{gm} \) is of course very good. It is worth noting that the use of quasi-static simulation models would almost certainly have lead to an unstable design.

**Linearity.** It is important to at least roughly determine the linear range of the transconductor, in order to assess its usability in the present design. We start with the consideration that in an active filter designed for maximum dynamic range, the maximum signal amplitude at any filter node must have the same value for all nodes. In the case of an active LC parallel pair, this maximum is reached at the same (resonant) frequency \( \omega_r = 1/\sqrt{LC} = g_m/C \). Thus, if the input voltages of a transconductor are \( V_{in+} = V_c + \Delta V, V_{in-} = V_c - \Delta V \) (\( V_c \) being the common-mode voltage), then

\[
\begin{align*}
V_{out+} &= V_c + g_m \Delta V/j\omega C = V_c + j\Delta V, \\
V_{out-} &= V_c - g_m \Delta V/j\omega C = V_c - j\Delta V,
\end{align*}
\]

since \( g_m/\omega C \) is unity at the resonant frequency. The above equations show that the first transistors to leave saturation are found in inverters \( I_3 \) and \( I_5 \). The saturation condition can be written as \( V_{ds} \geq V_{gs} - V_{th} \), with the usual meaning of the symbols. Here and in the following we focus on an nMOS transistor, the calculations being identical for a PMOS transistor. Using Eqs. (1)- (2), we obtain that saturation is enforced as long as

\[
\Delta V \geq \Delta V - V_{th}, \quad \Delta V \leq V_{th}/2.
\]

As a comparison, the transistors in inverters \( I_4 \) and \( I_5 \) work in saturation as long as \( \Delta V \leq V_{th}/\sqrt{2} \). Eq. (3) indicates that the threshold voltage \( V_{th} \) should not be too low, a rather uncommon demand in analog CMOS applications. A second condition for the proper behavior of the transconductor, however, is that no transistor leaves the strong inversion region, given by \( V_{gs} \geq V_{th} \). With \( V_{gs} = V_c - \Delta V \), and with \( V_c \) approximately equal to \( V_{dd}/2 \) (where \( V_{dd} \) is the voltage from the frequency-tuning circuit), we can rewrite the strong inversion condition as

\[
V_{dd}/2 - \Delta V \geq V_{th}, \quad \Delta V \leq V_{dd}/2 - V_{th}.
\]

Eqs. (3)-(4) give the same maximum \( \Delta V \) value for \( V_{th} = V_{dd}/3 \), in which case the linear range allowed by the power supply is as high as possible. For the CMOS process used in this work, \( V_{th} \) is about 0.8V, and the transconductor has been designed for \( V_{dd} = 2.5V \).
4. Measurements results

The filter was fabricated in a standard 0.6μm CMOS process. Fig. 5 shows a die photograph of the integrated circuit, which has dimensions 1050 μm × 510 μm. Measurements were performed with a power supply of about 2.5V, for a current consumption of 2.4mA. Twenty samples from two different runs were tested, always with very similar results.

The transfer function of the filter is shown in Fig. 6 (including the attenuation introduced by the output buffers). The passband gain is 0dB, the -3dB bandwidth is 1.05MHz (2.44MHz-3.49MHz), and the stop-band suppression is larger than 47dB for frequencies higher than 4MHz and lower than 2MHz. The group delay varies between 1.05μs and 1.8μs, giving a differential group delay of 0.75μs. The differential output noise level, measured over a 2MHz bandwidth, is 250μV rms.

The good linearity of the filter can be seen in Fig. 7, which shows an inter-modulation distortion level equal to the noise level for two in-band signals. The in-band spurious free dynamic range (SFDR) is 49dB. However, since the filter is narrow-band, a more interesting measurement is the SFDR in the presence of large out-of-band blockers. According to Fig. 8, the SFDR is at least 58dB for near blockers, and it levels at about 63dB for distant blockers. The level difference between IP3 and noise can be estimated from the relation SFDR = (2/3)(IP3 - Noise), which yields (IP3 - Noise) ≈ 80dB or higher for out-of-band signals. These figures show that the nonlinear behavior of the Bluetooth receiver is completely determined by the amplifiers and mixers preceding the filter.

Finally, the effect of large signals (1Vpp, or 3dB above the blocking level) at 2MHz, 3MHz (i.e. in-band), and 4MHz, respectively, on the filter bandwidth has been measured. The bandwidth deterioration (see Table 1, where most relevant features of the filter are listed) is only marginal.

5. Conclusions

An 18th order CMOS gm-C band-pass filter is presented, with a 3MHz center frequency and a 1MHz bandwidth. The filter shows high selectivity (-47dBc at 1MHz offset from the center frequency) and a high dynamic range (the spurious free dynamic range is 49dB for in-band signals, 63dB for distant out-of-band blockers) The filter is well suited for employment in the Bluetooth short-range radio receiver.

6. References

